REMARKS

This paper responds to the Office Action mailed on April 19, 2006.

None of the claims are amended or canceled. Claims 1-42 remain pending in this application.

Reservation of the Right to Swear Behind References

Applicant maintains the right to swear behind any references which are cited in a rejection under 35 U.S.C. §§102(a), 102(e), 103/102(a), and 103/102(e). Statements distinguishing the claimed subject matter over the cited references are not to be interpreted as admissions that the references are prior art.

Objection to the taking of Official Notice

The Office Action cites a single document (Bose et al.) to reject claims 2, 15, 18, 22, 30, 32, 33, 36, and 38 of the present application under 35 USC § 102(e) based on reasons that some of the specific features in these claims are *known in the art.* Applicant assumes that the Examiner is taking Official Notice in rejecting these claims because the Office Action offers no documents to support the rejection of the specific features in these claims. Applicant respectfully traverses the taking of Official Notice and, pursuant to M.P.E.P. § 2144.03, Applicant requests documents or an affidavit to support the rejection. In the absence of documents or an affidavit to support the rejection of claims 2, 15, 18, 22, 30, 32, 33, 36, and 38 Applicant requests reconsideration, withdrawal of the rejection, and allowance of these claims.

Notwithstanding the objection to the taking of Official Notice above, Applicant believes that claims 2, 15, 18, 22, 30, 32, 33, 36, and 38 are patentable over Bose et al. for the reasons presented below.

§102 Rejection of the Claims

Claims 1-30 and 34-38 were rejected under 35 USC § 102(e) as being anticipated by Bose et al. (U.S. Patent Publication No. 2004/0221185 A1, hereinafter referred to as Bose).

Applicant respectfully traverses for at least the reasons presented below.

Applicant believes that claims 1-30 and 34-38 are not anticipated by Bose because Applicant is unable to find Bose everything recited in each of the claims 1-30 and 34-38.

In general, Applicant believes that Bose teaches different things. Bose generates request signals 134 (FIG. 2) to power-on or power-off target units based on long term usage signals 144, short term usage signals 148, and idle history vector 149. Applicant is unable to find in Bose a teaching or fair suggestion that Bose generates request signals 134 to power-on or power-off target units based on software instructions in an instruction cache.

Detailed discussion of the teaching of Bose is presented below.

Independent claim 1

Independent claim 1 recites, among other things, that "the potentially needed functional unit is identified based on a determination of whether the potentially needed functional unit is operable to execute at least one software instruction stored within an instruction cache". Applicant believes that claim 1 is not anticipated by Bose because Applicant is unable to find everything recited in each of the claim 1.

The Office Action asserts that Bose, paragraph 40, line 1 through paragraph 41, line 5, teaches "the potentially needed functional unit is identified based on a determination of whether the potentially needed functional unit is operable to execute at least one software instruction stored within an instruction cache", as claimed in claim 1. Applicant respectfully disagrees.

Paragraph 40, line 1 through paragraph 41, line 5 describes current-cycle machine state vectors at input 132 (FIG. 1). These vectors at input 132 are used by a prediction logic 130 (FIG. 1) to generate request signals 134 to "wakeup" (power-on) or shutdown (power-off) target units (or functional units, as called by the Office Action). In FIG. 2, Bose provides a unit utilization vector output (UV) 142 based on vectors at input 132 from FIG. 1 (see Bose, paragraphs 42, lines 1-11). Bose teaches that UV 142 is used by a gating request control unit (GRCU) 150 to *determine which target units are already powered-on or powered-off* (see Bose, paragraph 44, lines 1-3). Applicant is unable to find in Bose a teaching or fair suggestion of how vectors at input 132 (FIG. 1) or UV 142 (FIG. 2) can be used by prediction logic 130 or by GRCU 150 to make a determination of whether the potentially needed target units of Bose is operable to execute at least one software instruction stored within an instruction cache such as an instruction

cache 102 of FIG. 1 of Bose. In contrast, claim 1 recites that "the potentially needed functional unit is identified based on a determination of whether the potentially needed functional unit is operable to execute at least one software instruction stored within an instruction cache". Accordingly, Applicant requests reconsideration, withdrawal of the rejection, and allowance of claim 1.

Dependent claims 2-14

Dependent claims 2-14 depend from claim 1 and recite the things of claim 1. Thus, Applicant believes that claims 2-14 are not anticipated by Bose for at least the reasons presented above regarding claim 1, plus the additional things recited in claims 2-14.

For example, regarding claims 3 and 4, Applicant is unable to find in Bose that instruction cache 102 (FIG. 1) can be used either as a conventional cache or a trace cache

In another example, regarding claim 5, Applicant is unable to find in Bose that how vector at input 132 is generated and stored, and how vector at input 132 of Bose can be used for identifying a set of functional units that are operable to execute the one or more software instructions and for identifying the potentially needed functional unit based on vector at input 132.

In another example, regarding claim 6, Applicant is unable to find in Bose how signals 134 can be used for indicating power status information for a set of functional units, wherein the power status information indicates whether a functional unit, within the set of functional units, has a present power level that places the functional unit in an operable power state or a low power state.

In another example, regarding claims 7 and 8, Bose teaches a counter 168 for counting "duration" of active or idling of a unit. Applicant is unable to find in Bose that counter 168 is used for "incrementing a use counter for a functional unit when a software instruction is fetched into the instruction cache, and when the functional unit is operable to execute at least part of the software instruction" and for "decrementing the use counter for the functional unit when the software instruction is eliminated from the instruction cache".

In another example, regarding claims 9-12, Bose teaches a processor 100 including a prediction logic 130 (FIG. 1 and FIG. 2). However, Applicant is unable to find in Bose that

processor 100, including prediction logic 130, can be used to perform the things that are recited in claims 9-12, as proposed by the Office Action.

In another example, regarding claim 14, Applicant is unable to find in Bose (paragraphs 28 and 42) "determining a selected operable power level from one of multiple operable power levels, wherein the selected operable power level is selected based on an expected result latency" and "initiating the power increase to the selected operable power level.

Accordingly, Applicant requests reconsideration, withdrawal of the rejection, and allowance of claims 2-14.

Independent claim 15

Applicant believes that independent claim 15 is not anticipated by Bose because Applicant is unable to find in Bose everything recited in claim 15.

The Office Action asserts that Bose teaches, in paragraph 39, lines 1-24, "fetching one or more lines of software instructions into an instruction cache, which is accessible to a processing engine", as claimed in claim 15. Applicant disagrees. Paragraph 39, lines 1-24 states, in part:

> "So, during each valid fetch cycle machine instructions are fetched **from** the ICACHE 102 based on an instruction fetch address from IFAR 104". (Emphasis added).

Thus, in the statement above, Bose teaches that cycle machine instructions are fetched "from" the ICACHE 102. In contrast, claim 15 recites fetching one or more lines of software instructions "into" (not from) an instruction cache.

The Office Action also asserts that Bose teaches, in paragraph 40, line 1 through paragraph 41, line 4, and paragraph 42, "identifying potentially needed functional units as functional units that are operable to execute at least one software instruction stored within the instruction cache, wherein a functional unit includes a portion of hardware, which is operable to perform a function in response to special instructions received from the processing engine", as also claimed in claim 15. Applicant disagrees. Paragraphs 40, 41, and 42 of Bose teach a prediction logic unit 130. As discussed above regarding claim 15, Bose teaches that UV 142 (FIG. 2), which is generated from vectors at input 132, is used by a gating request control unit

(GRCU) 150 of prediction logic 130 to *determine which target units are already powered-on or powered-off* (see Bose, paragraph 44, lines 1-3). Applicant is unable to find in Bose a teaching or fair suggestion of how vectors at input 132 (FIG. 1) or UV 142 (FIG. 2) can be used by prediction logic 130 or by GRCU 150 in "identifying potentially needed functional units as functional units that are operable to execute at least one software instruction stored within the instruction cache", as claimed in claim 15.

Further, Bose, paragraph 42, lines 18-21 states:

> "Each immediate power up vector 148 is a m-bit binary string that identifies which of the m downstream receiving execution units to turn on within the next few cycles".

Thus, in the statement above, vector 142 identifies which of execution units to turn on within the next few cycles. However, Applicant is unable to find in the statement above, a teaching or fair suggestion of how vector 148 is generated so that prediction logic 130 can *identifies* potentially needed functional units as functional units that are operable to execute at least one *software instruction stored within the instruction cache*, as claimed in claim 15.

The Office Action further asserts that Bose teaches, in paragraph 40, lines 1-8, and paragraph 42, "identifying unneeded functional units as functional units that are not operable to execute a software instruction stored within the instruction cache", as further claimed in claim 15. Applicant disagrees. Paragraph 40, lines 1-8 states, in part:

> "when a (relatively) **long stretch of idleness** is identified for a unit, a "power off" or "sleep" request is issued to shut down that unit, placing it in a dormant state". (Emphasis added).

Thus, in the statement above, Bose teaches shutting down a unit when a (relatively) *long stretch of idleness* is identified for that unit. Applicant is unable to find Bose a teaching or fair suggestion that Bose teaches shutting down a unit or units when the units are identified as units that are *not operable to execute a software instruction stored within the instruction cache.* In contrast, claim 15 recites "identifying unneeded functional units as functional units that are not operable to execute a software instruction stored within the instruction cache".

The Office Action continues to assert that Bose teaches, in paragraph 37, lines 20-28 "initiating a power increase for selected ones of the potentially needed functional units that are in a low power state", and "initiating a power decrease for selected ones of the unneeded functional units that are in an operable power state", as a further claimed in claim 15. Applicant disagrees. Paragraph 37, lines 20-28 states:

> "In addition, unit-level activity prediction logic 130 receives a current-cycle machine state vector 132 as input and provides request signal(s) 134 that **"wake up" target units or initiate "sleep"** or "power-down" to selectively shut down a target unit **in anticipation of a (relatively) long idle stretch for that unit**. Each and any of units 102, 104, 106, 108, 110, 112, 114, 116, 118, 120, 122, 124, 126 and/or 128 may be designated target units.". (Emphasis added).

Thus, in the statement above, Bose teaches that prediction logic 130 can "wake up" target units. However, Applicant is unable to find how Bose is unable to find a teaching or fair suggestion of how prediction logic 130 can initiate a power increase for *selected* ones of the *potentially needed functional units that are in a low power state,* as claimed in claim 15. As also stated in the statement above, Bose teaches that prediction logic 130 can shut down a target unit *in anticipation of a (relatively) long idle stretch for that unit.* Applicant is unable to find in Bose a teaching or fair suggestion that prediction logic 130 can initiate a power decrease for *selected* ones of the unneeded functional units *that are in an operable power state,* as claimed in claim 15.

Based on all of the reasons presented above, Applicant believes that claim 15 is not anticipated by Bose. Accordingly, Applicant requests reconsideration, withdrawal of the rejection, and allowance of claim 15.

Dependent claims 16-20

Dependent claims 16-20 depend from claim 15 and recite the things of claim 15. Thus, Applicant believes that claims 16-20 are also not anticipated by Bose for at least the reasons presented above regarding claim 15, plus the additional things recited in claims 16-20.

Accordingly, Applicant requests reconsideration, withdrawal of the rejection, and allowance of claims 16-20.

Independent claim 21

Independent claim 21 recites, "identifying a potentially needed functional unit as a functional unit that is operable to execute at least one software instruction stored within an instruction cache" and "initiating a power increase for the potentially needed functional unit, if the potentially needed functional unit has a present power level that is lower than an operable power level". For at least the reasons presented above regarding claim 1, Applicant is unable to find in Bose "identifying a potentially needed functional unit as a functional unit that is operable to execute at least one software instruction stored within an instruction cache" and "initiating a power increase for the potentially needed functional unit, if the potentially needed functional unit has a present power level that is lower than an operable power level". Accordingly, Applicant requests reconsideration, withdrawal of the rejection, and allowance of claim 1.

Dependent claims 22-25

Dependent claims 22-25 depend from claim 21 and recite the things of claim 21. Thus, Applicant believes that claims 22-25 are also not anticipated by Bose for at least the reasons presented above regarding claim 21, plus the additional things recited in claims 22-25. Accordingly, Applicant requests reconsideration, withdrawal of the rejection, and allowance of claims 22-25.

Independent claim 26

Independent claim 26 recites, among other things, one or more power controllers, which are operable to control whether or not an operable power level or a low power level is provided to selected ones of the one or more functional units, "based on whether or not selected ones of the one or more functional units are operable to execute at least one software instruction stored within the instruction cache". For at least the reasons presented above regarding claim 1, Applicant is unable to find in Bose one or more power controllers, which are operable to control whether or not an operable power level or a low power level is provided to selected ones of the

one or more functional units, "based on whether or not selected ones of the one or more functional units are operable to execute at least one software instruction stored within the instruction cache". Accordingly, Applicant requests reconsideration, withdrawal of the rejection, and allowance of claim 26.

Dependent claims 27-30 and 34-38

Dependent claims 27-30 and 34-38 depend from claim 1 and recite the things of claim 1. Thus, Applicant believes that claims 27-30 and 34-38 are not anticipated by Bose for at least the reasons presented above regarding claim 1, plus the additional things recited in claims 27-30 and 34-38.

For example, regarding claim 28, Applicant is unable to find in Bose that at least one of the target units that is to be "wake up" or put to "sleep" includes an external functional unit, which is "not" located on a "same chip" as the processing engine of Bose.

§103 Rejection of the Claims

Claims 31-33 and 39-42 were rejected under 35 USC § 103(a) as being unpatentable over Bose in view of Theis (U.S. Patent Publication No. 2005/0251621 A1).

Applicant respectfully traverses for at least the reasons presented below.

Dependent claims 31-33

Dependent claims 31-33 depend from claim 26 and recite the things of claim 26. Thus, Applicant believes that claims 31-33 are patentable over Bose and Theis because Applicant is unable to find in Bose and Theis everything recited in claim 31-33. For example, Applicant is unable to find in Bose and Theis, whether considered individually or in the proposed combination, one or more power controllers, which are operable to control whether or not an operable power level or a low power level is provided to selected ones of the one or more functional units, "based on whether or not selected ones of the one or more functional units are operable to execute at least one software instruction stored within the instruction cache". Further, Applicant believes that Bose and Theis teach different things. Therefore, Applicant believes that claims 31-33 are patentable over Bose and Theis because Applicant cannot find a

motivation to combine the different teachings of Bose and Theis as proposed by the Office Action. Based on all of the reasons presented herein, Applicant believes that claims 31-33 are patentable over Bose and Theis, whether considered individually or in the proposed combination. Accordingly, Applicant requests reconsideration, withdrawal of the rejection, and allowance of claims 31-33.

Independent claim 39

Independent claim 39 recites, among other things, "a mechanism to sequentially access the storage locations within the array using an enable signal, which has a value that results from shifting information within one or more shift registers". Applicant believes that claim 39 is patentable over Bose and Theis because Applicant is unable to find in Bose and Theis everything recited in claim 39.

The Office Action admits that Bose fails to disclose a mechanism to sequentially access the storage locations within the array "using an enable signal, which has a value that results from shifting information within one or more shift registers".

The Office Action relies on Theis, paragraph 218, and asserts that Theis teaches a mechanism to sequentially access the storage locations within the array "using an enable signal, which has a value that results from shifting information within one or more shift register", as claimed in claim 39. Applicant disagrees. Paragraph 218 of Theis describes a movement of a pointer in a circular stack. Applicant is unable to find in Theis a mechanism to sequentially access the storage locations within the array "using an enable signal, which has a value that results from shifting information within one or more shift registers".

Further, Applicant believes that Bose and Theis teach different things. Therefore, Applicant believes that claim 39 is patentable over Bose and Theis because Applicant cannot find a motivation to combine the different teachings of Bose and Theis as proposed by the Office Action.

Based on all of the reasons presented herein, Applicant believes that claim 39 is patentable over Bose and Theis, whether considered individually or in the proposed combination. Accordingly, Applicant requests reconsideration, withdrawal of the rejection, and allowance of claim 39.

Dependent claims 40-42

Dependent claims 40-42 depend from claim 39 and recite the things of claim 39. Thus, Applicant believes that claims 40-42 are patentable over Bose and Theis for at least the reasons presented above regarding claim 39, plus the additional things recited in claims 40-42.

For example, regarding claims 40 and 41, Applicant is unable to find in Bose and Theis, whether considered individually or in the proposed combination, "a plurality of first latches, within which a first portion of the enable signal is stored, and wherein the first portion of the enable signal is used to activate a selected word line within the array" and "a plurality of second latches, within which a second portion of the enable signal is stored, wherein the second portion of the enable signal is used to select a portion of the selected word line".

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney ((612) 373-6969) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexendria, VA 22313-1450 on this 21st day of August 2006

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